



US-PAT-NO: 5610852

DOCUMENT-IDENTIFIER: US 5610852 A

TITLE: Ferroelectric memory and method for controlling operation of the same

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Detailed Description Text - DETX (4):

The control signal lines 28A and 28B are maintained at the high level in a standby condition, and brought to the low level before or at the same time as the selection signal lines 11A and 13A are brought to the high level, so that the capacitor is reverse-coupled against noises outputted from the memory cell, thereby absorbing the noises. The electric charge amount of noise absorbed can be modified by adjusting the size of the capacitor and the voltage level of the high level and the low level of the control signal lines 28A and 28B. Accordingly, these parameters can be set to a suitable value in view of the magnitude of the noise outputted from the memory cell.

Koike et al. [45] Date of Patent: Mar. 11, 1997

[34] FERROELECTRIC MEMORY AND METHOD FOR CONTROLLING OPERATION OF THE SAME 5,433,786 10/1995 Takeuchi et al. 362/145  
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[21] Appl. No.: 882,619

[22] Filed: Jan. 4, 1996

[30] Foreign Application Priority Data  
Jan. 4, 1995 JP7 Japan 7-000063

[31] Int. Cl.<sup>6</sup> G11C 11/22

[32] U.S. Cl. 365/148; 365/206

[38] Field of Search 365/208, 149, 150

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[57] ABSTRACT  
In a ferroelectric memory, when data is read out from a memory cell, a variation absorbing circuit minimizes a variation of the voltage on the pair of data signal lines caused by factor other than the current caused due to the polarization of the ferroelectric capacitor. Thus, a voltage not smaller than the coercive voltage can be applied between the opposing electrodes of the ferroelectric capacitor, with the result that a sufficient read-out signal voltage can be obtained.

38 Claims, 33 Drawing Sheets